(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 554 063 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
28.06.2000 Bulletin 2000/26

(51) Int. Cl.[7]: **H01L 27/12**

(21) Application number: **93300572.0**

(22) Date of filing: **27.01.1993**

(54) Method of producing a CMOS inverter on a soi-substrate with a SIMOX technique

Verfahren zur Herstellung eines CMOS-Inverters auf einem SOI-Substrat mit Hilfe einer SIMOX Technik

Procédé pour la fabrication d'un inverteur du type CMOS sur un substrate du type soi avec une technique SIMOX

(84) Designated Contracting States:
DE FR GB

(30) Priority: **31.01.1992 JP 4049692**

(43) Date of publication of application:
04.08.1993 Bulletin 1993/31

(73) Proprietor:
CANON KABUSHIKI KAISHA
Tokyo (JP)

(72) Inventors:
- **Inoue, Shunsuke,**
  c/o Canon Kabushiki Kaisha
  Tokyo (JP)
- **Koizumi, Toru,**
  c/o Canon Kabushiki Kaisha
  Tokyo (JP)
- **Miyawaki, Mamoru,**
  c/o Canon Kabushiki Kaisha
  Tokyo (JP)
- **Sugawa, Shigetoshi,**
  c/o Canon Kabushiki Kaisha
  Tokyo (JP)

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
High Holborn
2-5 Warwick Court
London WC1R 5DJ (GB)

(56) References cited:
US-A- 4 409 724

- **PATENT ABSTRACTS OF JAPAN vol. 12, no. 402 (E-673)(3249) 25 October 1988**
- **K. Hashimoto et al., IEDM Technical Digest, pp 672-675, 1985**
- **H. Onada et al., IEDM Technical Digest, pp 680-683, 1985**
- **K. Anzai et al., IEDM Technical Digest, pp 796-799, 1984**
- **B-Y. Tsaur et al., IEDM Technical Digest, pp 812-815, 1984**
- **A.J. Auberton Herve et al., IEDM Technical Digest, pp 808-811, 1984**

EP 0 554 063 B1

Printed by Xerox (UK) Business Services
2.16.7 (HRS)/3.6

Description

[0001] This invention relates to a method of producing thin-film CMOS inverter circuit and to a method of producing the active matrix substrate of an active matrix liquid crystal display device having the inverter circuit as a peripheral drive circuit and which also includes an active matrix display portion having PMOS transistor pixel switches.

[0002] With the recent rapid progress of semiconductor technology, there has been a demand for smaller, high-speed and small-power-consumption semiconductor devices and apparatuses using such devices. The development of complementary MOS (CMOS) inverters using P-channel and N-channel enhancement type MOS field effect transistors (FET) as load and inverter devices among such apparatuses is being further promoted because the power consumption of this type of inverter is very small, although a complicated manufacturing process is required.

[0003] Thin film transistor silion-on-insulator complementary MOS circuits and methods for producing the same, are disclosed, for example, in each of the following publications (hereinafter referred to as publications (1) to (5)):

1. K. Anzai, et al, "Fabrication of high speed 1 micron FIPOS/CMOS", in IEDM Technical Digest, pp 796-799, 1984;
2. A.J. Auberton Herve, et al, "Device performances of a submicron SOI technology", in IEDM Technical Digest, pp 808-811, 1984;
3. B-Y. Tsaur, et al, "Merged CMOS Bipolar Technologies and Microwave MESFETs utilising zone-melting-recrystallised SOI films", in IEDM Technical Digest, pp. 812-815, 1984;
4. K. Hashimoto, et al, "Characteristics of submicrometer CMOS transistors in implanted-buried-oxide SOI films", in IEDM Technical Digest, pp 672-675, 1985; and
5. H. Onoda, et al, "Si-gate CMOS devices on a Si/CaF_2/Si structure", in IEDM Technical Digest, pp 680-683, 1985.

[0004] In particular, publication (4) discloses PMOS and NMOS thin film SOI transistors produced by implanting oxygen ions. As described therein oxygen ions were implanted with a dose of $2x10^{18}$ cm^{-2} and energies of 150 - 180 keV, and this was followed by anneal treatment. An implanted buried oxide layer of thickness 400nm was produced by this means.

[0005] By comparison, publication (1) discloses production of CMOS inverters using oxidised porous silicon as means of the SOI insulation. An insulation layer of thickness 8μm is reported therein. This is stated to suppress back channel leakage current for the NMOS transistors. A low junction leakage level of $1x10^{-12}$A was achieved.

[0006] Publication (2) discloses CMOS ring oscillator manufacture using an SOI substrate on which the active Si layer was formed by laser zone-melting recrystallisation of Si deposited on an oxide layer on the surface of a Si monocrystalline bulk substrate. In the construction produced a back interface leakage event for NMOS transistors as low as 0.2 pA/channel width was achieved with an oxide layer of thickness 200 nm. This document identifies back-gate parasitic transistors in which the channels are coupled to the monocrystalline bulk substrate with insulated gate.

[0007] Fig. 1(a) shows an example of a CMOS inverter in section. A transistor 16 is an NMOS transistor while a transistor 17 is a PMOS transistor. The transistors 16 and 17 are formed on a substrate while being insulated by a base insulation layer 2 and separated from each other by SiO_2 3. The MOS transistor 16 is constituted of an N^+ drain 5, a P-channel region 10, an N-type field limiting regions 12, 12', a gate insulation film 8, a gate electrode 9, a source electrode 14, and a drain electrode 15. The gate electrode is ordinarily formed of a polycrystalline Si, and the source and drain electrodes are formed of Al.

[0008] The PMOS transistor 17 is constituted of a P^+ drain 6, a P^+ source 7, N-channel region 11, a P-type field limiting regions 13, 13', a gate insulation film 8', a gate electrode 9', a source electrode 14', and a drain electrode 15'.

[0009] Fig. 1(b) is an equivalent circuit diagram of the above-described CMOS inverter. As illustrated, the drain electrode 15 of the NMOS transistor 16 and the drain electrode 15' of the PMOS transistor 17 are connected to a common output electrode. An output voltage at this output electrode is represented by V_{out}. The source electrode 14 of the NMOS transistor 16 is connected to a low-voltage power supply, while the source electrode 14' of the PMOS transistor 17 is connected to a high-voltage power supply. The voltages of these power supplies are represented by V_{SS} and V_{DD}. The substrate 1 forms gate electrodes of parasitic MOS transistors with respect to the NMOS transistor 16 and the PMOS transistor 17. That is, a parasitic PMOS transistor having a gate insulation layer corresponding to the base insulation layer 2, a channel region corresponding to the region 11, and a source and a drain corresponding to the drain 6 and the source 7 is formed, while a parasitic NMOS transistor having a gate insulation layer corresponding to the base insulation layer 2, a channel region corresponding to the region 10, and a source and a drain corresponding to the source 4 and the drain 5 is formed. V_{back} in Fig. 1(b) represents a voltage input to these parasitic CMOS transistors.

[0010] Fig. 9 shows input-output characteristics of a conventional CMOS inverter. In the case of conventional CMOS inverters, it is difficult to increase the absolute value of threshold voltages of parasitic MOS transistors. If the threshold values of the parasitic NMOS and PMOS transistors are V_{thbn}, and V_{thbp}, respectively, $V_{thbn} - V_{thbp}$ (the threshold value of the PMOS transistor being ordinarily negative) $> V_{DD} - V_{SS}$.

[0011] With respect to any value of V_{back}, the parasitic NMOS or PMOS transistor can operate. As shown in Fig. 9,

in the case where V_{in} becomes closer to V_{DD} when V_{back} is about zero, the parasitic PMOS transistor is operating and a leak current through the PMOS transistor inhibits the output from completely dropping to V_{SS}. On the other hand, in the case where V_{in} becomes closer to V_{SS} when V_{back} is about 3 V, the parasitic NMOS transistor is operating and a leak current through the NMOS transistor inhibits the output from completely rising to V_{DD}.

[0012] As described above, a leak current flows by the operation of a parasitic CMOS transistor in the conventional CMOS inverter, resulting in failure to obtain an ideal input-output characteristic of the transistor.

[0013] US-A-4409724 discloses a semiconductor device in which a CMOS transistor is formed on a thick quartz substrate. A polysilicon layer is disposed on the substrate which is then patterned to provide a plurality of islands. The islands are subjected to a laser annealing treatment at an intensity sufficient to cause recrystalisation. The polysilicon material in the islands is converted by the laser annealing to crystalline silicon having an enhanced electron mobility characteristics. A pair of islands of polycrystalline semiconductor material as annealed by energy from a focused energy source are then formed into a CMOS transistor.

[0014] WO-A-8902095 discloses a liquid crystal display device with a SOI substrate having an epitaxial silicon layer lying over an implant generated dielectric layer. MOS device and capacitor elements used to activate the display are formed and interconnected in the epitaxial silicon. The implant generated dielectric layer and the silicon substrate also serve as capacitor elements, thereby simplifying the structure and fabrication of the display device and providing improved operation through improved isolation of the MOS device elements formed in the epitaxial silicon from the substrate.

[0015] JP-A-63-142851 discloses a semiconductor device in which a conductive layer is provided under an FET with an insulating layer therebetween in order to drive the FET with increased stability. The insulating layer provided between the FET and the conductive layer has a thickness of between 2×10^{-7} and 6×10^{-7} meters. When the potential of the conductive layer is grounded the conductive layer and channel regions of the FET have a large capacitance through the insulating film thus inhibiting the potential fluctuation of the channel regions due to the modulation of pulses having high frequency thus preventing the malfunction of the circuit.

[0016] In accordance with the present invention, there are provided methods of producing a thin-film CMOS inverter circuit in accordance with claims 1 and 2, respectively. A method of producing the active matrix substrate of an active matrix liquid crystal display device and or either of these methods is defined in claim 3 attached.

[0017] An embodiment of the present invention produces an inverter circuit free from the above-described problem and a liquid crystal display using the inverter circuit.

[0018] The thin-film CMOS inverter circuit produced in accordance with the present invention has an insulation layer thick enough to solve the above-described problem.

[0019] In the accompanying drawings:

Fig. 1(a) is a cross-sectional view of an example of an inverter of an inverter circuit produced in accordance with the present invention;
Fig. 1(b) is a equivalent circuit diagram of the inverter shown in Fig. 1;
Fig. 2 is a diagram of an input-output characteristic of a CMOS inverter of an inverter circuit produced in accordance with an embodiment of the present invention;
Fig. 3 is a diagram of film thickness-threshold value characteristics of a parasitic NMOS transistor;
Fig. 4 is a diagram of film thickness-threshold value characteristics of a parasitic PMOS transistor;
Fig. 5 is a diagram of a relationship between the threshold value and the film thickness of the parasitic MOS transistors;
Fig. 6(a) is a diagram of a SIMOX process practiced in accordance with a preferred (second) embodiment of the present invention;
Fig. 6(b) is a oxygen concentration profile of the process of the preferred (second) embodiment;
Fig. 7 is an illustration of a matrix substrate in a state of production by laser annealing ;
Fig. 8 is a cross-sectional view of an active matrix produced according to an embodiment of the present invention; and
Fig. 9 is a diagram of input-output characteristics of a conventional CMOS inverter.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] The present invention will be described below in detail.

[0021] As described above, in accordance with the principle of the operation of a CMOS inverter, a condition necessary for the existence of a value of V_{back} with which parasitic NMOS and PMOS transistors cannot operate is $V_{SS} + V_{thbn} < V_{DD} + V_{thbp}$.

[0022] V_{thbn} and V_{thbp} can be expressed as shown below.

$$V_{thbn} = + (Q_{BN}/C_{BOX}) + 2\phi_{FN} + V_{FB}$$

$$Q_{BN} = \sqrt{2q\epsilon N_{CN}(2\phi F_N)}$$

$$V_{FB} = - qQ_{SS}/C_{BOX} - 0.88V$$

$$V_{thbp} = - (Q_{BP}/C_{BOX}) - 2\phi_{FP} + V'_{FB}$$

$$Q_{BP} = \sqrt{2q\epsilon N_{CP}(2\phi F_P)}$$

$$V'_{FB} = - qQ_{SS}/C_{BOX} + 0.15V$$

C_{BOX}: the capacity per unit area of the base insulation layer (F/cm^2)
q: elementary electric charge
N_C: a channel impurity concentration
ϕ_{FN}, ϕ_{FP}: psuedo Fermi potentials of the NMOS and PMOS transistors
$\phi_F = (kT/q)\ln(N_C/n_i)$

k: Boltzmann's constant
T: absolute temperature
n_i: an intrinsic carrier density of Si

V_{FB}: a flat band voltage

[0023] Therefore,

$$V_{thbn} - V_{thbp} = (Q_{BN} + Q_{BP})/C_{BOX} + 2\phi_{FN} + 2\phi_{FP} - 1.03.$$

[0024] Each of the Q_{BN}, Q_{BP} ϕ_{FN}, and ϕ_{FP} in the above has only one value if the impurity concentrations N_{cn} and N_{cp} are determined.

$$\text{Since } C_{BOX} = \epsilon_{BOX}/T_{BOX}$$

ϵ_{BOX}: a dielectric constant of the base insulation layer
T_{BOX}: the thickness of the base insulation layer,

only C_{BOX} in the above equation is changed with the thickness of the base insulation layer. Accordingly,

$$V_{thbn} - V_{thbp} = K_1 T_{BOX} + K_2$$

where

$$K_1 \equiv \varepsilon_{BOX}^{-1} (Q_{BN} + Q_{BP})$$

and

$$K_2 = 2\phi_{FN} + 2\phi_{FP} - 1.03.$$

$\therefore V_{DD} - V_{SS} < V_{thbn} - V_{thbp} = K_1 T_{BOX} + K_2$
$\therefore T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$

[0025] If the base insulation layer has a thickness such as to satisfy this equation, the absolute value of the threshold values can be increased so that occurrence of a leak current is prevented.

[0026] The thickness of an insulation layer in the conventional SIMOX substrate cannot be indefinitely increased. In accordance with the present invention, a monocrystal Si region is provided on a thick insulation layer by modified SIMOX (which may include subsequent epitaxial growth).

[0027] The present invention will be described with respect to Examples 3, 4, & 6 thereof, and other examples 1, 2, 5 of methods outside the scope of the present invention.

Example 1

[0028] A monocrystal Si thin film was formed by using a porous Si substrate member. A method of manufacturing this monocrystal Si thin film will be described below.

[0029] In the porous Si substrate member used, holes having a diameter of about 60 nm (600 Å) on an average are formed, which were observed through a transmission microscope. The density of the porous Si substrate is at most half that of monocrystal Si, but its monocrystal properties are maintained and a monocrystal Si layer can be formed on the porous layer by epitaxial growth. However, a rearrangement of internal holes takes place at 1,000°C or higher, and the characteristics of enhanced etching are thereby impaired. For this reason, a low-temperature growing method, such as a molecular beam epitaxial growth method, a plasma chemical vapor deposition (CVD) method, a thermal CVD method, a photo-CVD method, a bias sputtering method, or a liquid crystal growth method, is preferred as a method for growing the Si layer.

[0030] A method in which P-type Si is made porous and a monocrystal layer is thereafter grown by epitaxial growth will be described below.

[0031] First, a Si monocrystal substrate member is prepared and is processed by an anodization method using a HF solution to form a porous layer therein. While the density of monocrystal Si is 2.33 g/cm^3, the density of the porous Si can be changed in the range of 0.6 to 1.1 g/cm^3 by changing the HF solution concentration in the range of 20 to 50 % by weight. This porous layer can easily be formed into a P-type Si substrate member for a reason described below.

[0032] Porous Si was found in a process of studying electrolytic polishing of a semiconductor. In a dissolution reaction of Si in anodization, positive holes are required for anodization of Si in the HF solution. This reaction is expressed as follows.

$$Si + 2HF + (2 - n)e^+ \rightarrow SiF_2 + 2H^+ + ne^-$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (4 - \lambda)e^+ \rightarrow SiF_4 + 4H^+ + \lambda e^-$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

[0033] Symbols e^+ and e^- represent holes and electrons, respectively. Each of n and λ represents the number of holes, in the relevant equation, necessary for dissolving one Si atom. Porous Si is formed on condition that $n > 2$ or $\lambda > 4$.

[0034] From this fact, it can be said that P-type Si in which holes exist can easily be made porous.

[0035] On the other hand, it has been reported that high-density N-type Si can be made porous. Thus, a Si substrate member can be made porous irrespective of being P- or N-type.

[0036] Also, the density of the porous layer is a half or less of the original density, since many gaps are formed in the porous layer. Therefore the surface area is greatly increased relative to the volume. The chemical etching speed is thereby increased remarkably in comparison with the etching speed of the ordinary monocrystal layer.

[0037] Conditions for making monocrystal Si porous by anodization are shown below. A starting material of porous Si formed by anodization is not limited to monocrystal Si, and Si in other crystalline structures can be used.

Applied voltage: 2 (V)
Current density: 30 (mA • cm^{-2})
anodization solution: HF : H_2O : C_2H_5OH = 1 : 1 : 1
Time: 2.4 (hours)
Thickness of porous Si: 300 (μm)
Porosity: 56 %

[0038] Si is grown by epitaxial growth on porous Si formed in this manner, thereby forming a monocrystal Si thin film. The thickness of the monocrystal Si thin film is, preferably, 50 μm or less, more preferably, 20 μm or less.

[0039] A surface of the monocrystal Si thin film is then oxidized. A substrate member which is to finally form a main substrate is prepared and is attached to the oxide film in the monocrystal Si surface. Alternatively, a surface of monocrystal Si substrate member newly prepared is oxidized and is attached to the monocrystal Si layer on the porous Si substrate member. The reason for the provision of such an oxide film between the substrate member and the monocrystal Si layer is because an interface level generated from a base interface of a Si active layer with an oxide film can be smaller than, for example, an interface level from a base interface with a glass provided as a substrate member. It is possible to greatly improve characteristics of an electronic device by forming such an oxide film interface. Further, only a monocrystal Si thin film prepared by removing a porous Si substrate member by a selective etching process described later may be attached to a new substrate member. Two substrate members can be attached closely enough to prevent separation between them by the van der Waals force, if their surfaces are washed and thereafter brought into contact with each other at room temperature. However, the substrate members in this state are processed by a heat treatment in a nitrogen atmosphere at a temperature in the range of 200 to 900°C, preferably, 600 to 900°C.

[0040] An Si_3N_4 layer is formed as an etching prevention film by deposition over the entire surface of the two attached substrate members. Only the portion of the Si_3N_4 layer on the surface of the porous Si substrate member is then removed. Apiezon wax may be used instead of Si_3N_4. Thereafter, the porous Si substrate member is entirely removed by etching or other means. A semiconductor substrate having a thin monocrystal Si layer can be obtained in this manner.

[0041] A selective etching method for etching only the porous Si substrate member by non-electrolyte wet etching will be described below.

[0042] As an etching liquid having no etching effect with respect to crystalline Si but capable of selectively etching only porous Si, it is preferable to use hydrofluoric acid, buffered hydrofluoric acid of ammonium fluoride (NH_4F), hydrogen fluoride (HF) or the like, a liquid of a mixture of hydrofluoric acid or buffered hydrofluoric acid and hydrogen peroxide solution, a liquid of a mixture of hydrofluoric acid or buffered hydrofluoric acid and alcohol, or a liquid of a mixture of hydrofluoric acid or buffered hydrofluoric acid, hydrogen peroxide solution and alcohol. The substrate members attached to each other undergo etching by being wetted with such an etching liquid. The etching speed depends upon the concentration of hydrofluoric acid, buffered hydrofluoric acid and hydrogen peroxide in the solution and upon the temperature. By the addition of the hydrogen peroxide solution, the oxidation of Si is promoted and the reaction speed is increased in comparison with an etching liquid to which no hydrogen peroxide solution is added. Further, the reaction speed can be controlled by changing the proportion of the hydrogen peroxide solution. By the addition of alcohol, bubbles of a reaction product gas can be instantly removed from the etched surface without agitation, and the porous Si can be etched uniformly and efficiently.

[0043] The HF concentration in buffered hydrofluoric acid is set in the range of, preferably, 1 to 95 %, more preferably, 1 to 85 %, and further preferably, 1 to 70 % by weight of the etching liquid.

[0044] The NH_4F concentration in buffered hydrofluoric acid is set in the range of, preferably, 1 to 95 %, more preferably, 5 to 90 %, and further preferably, 5 to 80 % by weight of the etching liquid.

[0045] The HF concentration is set in the range of, preferably, 1 to 95 %, more preferably, 5 to 90 %, and further preferably, 5 to 80 % by weight of the etching liquid.

[0046] The H_2O_2 concentration is set in the range of, preferably, 1 to 95 %, more preferably, 5 to 90 %, and further preferably, 10 to 80 % by weight of the etching liquid, and is set in a range such that the above-described effect of hydrogen peroxide solution can be attained.

[0047] The alcohol concentration is set in the range of, preferably, 80 % or less, more preferably, 60 % or less, and further preferably, 40 % or less by weight of the etching liquid, and is set in a range such that the above-described effect of alcohol can be attained.

[0048] The temperature is set in the range of, preferably, 0 to 100°C, more preferably, 5 to 80°C, and further preferably, 5 to 60°C.

[0049] The alcohol used may comprises ethyl alcohol, isopropyl alcohol and the like, i.e., alcohols which entail no considerable problem in the manufacturing process in practice and which ensure the above-described alcohol addition effect.

[0050] In the semiconductor substrate obtained in this manner, a thin large-area layer of monocrystal Si equivalent to the ordinary Si wafer is formed flat and uniformly to cover the entire area on the substrate.

[0051] A monocrystal Si thin film, such as the one described in detail in the specification of European Patent Laid-Open Publication No. 469630, can be specifically used as the above-described monocrystal Si thin film.

[0052] In this example, a SiO_2 film having a thickness of 1 μm (10,000 Å) was formed on a monocrystal Si substrate, and was attached to a monocrystal Si thin film to form a base insulation layer. A CMOS inverter such as that shown in Fig. 1 was manufactured by using this base insulation layer. The method of setting the above-mentioned film thickness will be described below.

[0053] Fig. 3 shows film thickness (T_{BOX})-threshold value (V_{thbn}) characteristics of a parasitic NMOS transistor with Q_{SS} (fixed positive charge on the base insulation layer) (cm^{-2}) used as a parameter. The density in the channel region

was set to 1×10^{16} cm^{-3}.

[0054] Fig. 4 shows film thickness-threshold value (V_{thbp}) characteristics of a parasitic PMOS transistor with Q_{SS} used as a parameter. The density in the channel region was set to 5×10^{15} cm^{-3}.

[0055] Fig. 5 shows a relationship between the film thickness and the threshold value difference V_{thbn} - V_{thbp} between the two transistors on the basis of the data shown in Figs. 3 and 4 with respect to the channel densities of 1×10^{16} cm^{-3} and 5×10^{15} cm^{-3}.

[0056] As described above, for the existence of a value of V_{back} with which the parasitic NMOS and PMOS transistors cannot operate, at least V_{DD} - V_{SS} < V_{thbn} - V_{thbp} must be satisfied. The graph of Fig. 5 is formed by using, as a parameter, allowable values of currents flowing in gate voltage ranges below the threshold values. In Fig. 1, the relationship between V_{thbn} - V_{thbp} and T_{BOX} is shown with respect to a current of 1 μm flowing when V_{back} = V_{thbn}, V_{thbp}, a current down by a factor of 10^2 therefrom (allowable current = 10 μA), a current down by a factor of 10^4 (allowable current = 10 nA), and a current down by a factor of 10^6 (allowable current = 100 pA). There is no influence of Q_{SS} upon the relationship shown in this graph.

[0057] In this example, a base insulation layer thickness T_{BOX} = 1 μm (10,000 Å) was determined from Fig. 5 under conditions: V_{DD} - V_{SS} = 14 V, an allowable current of 100 pA, and a margin of 5 V between the threshold value difference and V_{DD} - V_{SS}.

[0058] Fig. 2 shows an input-output characteristic of this CMOS inverter. Input-output values closer to an ideal characteristic were exhibited with respect to V_{DD} = 8 V, V_{SS} = - 6 V, and V_{back} = 3 V. This CMOS inverter can be used in a driving circuit having a high power supply voltage, 14 V.

Example 2

[0059] A semiconductor device was manufactured in the same manner as Example 1 except that a base insulation layer was formed so as to have a three-layer structure formed of 800 nm (8,000 Å) thick layer of SiO_2, a 50 nm (500 Å) thick layer of SiN, and a 100 nm (1,000 Å) thick layer of SiO_2. The thickness of this three-layer film corresponds to about 925 nm (9,250 Å) in terms of the thickness of the SiO_2 single layer structure as determined by conversion with respect to the dielectric constant. In this embodiment, SiN was deposited by a low pressure CVD method. Alternatively, SiN may be formed by being nitrized by rapid thermal annealing at 1,000°C after SiO_2 deposition.

[0060] In a case where there is a need to partially remove the Si substrate by etching on the back side thereof, for example, for the purpose of forming a transparent portion such as that of a display portion of a liquid crystal display, etching can easily be stopped since the SiN layer acts as a suitable stopper, and cutting-out can be performed by uniform back-side etching.

[0061] The operation at V_{DD} - V_{SS} = 14 V was substantially possible, although the threshold values of the parasitic MOS transistors were slightly reduced in comparison with Example 1.

Example 3 (1st Embodiment)

[0062] Conventionally, a SIMOX substrate is manufactured by a method of injecting, ordinarily, 3 to 5 separated shots of an amount of oxygen ions of 4×10^{17} to 2.4×10^{18} cm^{-2} with acceleration energy of 150 to 300 keV, and thereafter performing a heat treatment at 1,100 to 1,250°C for 2 to 20 hours.

[0063] In this embodiment, oxygen ions were injected by double-charging using a charge twice as large as the ordinary charge, while an average ion injection range (ion injection depth) R_p = 800 nm (8,000 Å) and a dispersion of ion injection range ΔRp = 400 nm (4,000 Å) were set. SiO_2 film having a thickness of 1 μm (10,000 Å) was thereby formed. A CMOS inverter similar to that in accordance with Example 1 was manufactured by using this SIMOX substrate. The CMOS inverter obtained had no leak and had an improved characteristic.

Example 4 (2nd Embodiment)

[0064] A SIMOX substrate was manufactured by changing energy for oxygen ion injection by three steps as shown in Fig. 6(a). That is, oxygen ions were injected under conditions: The plant energy of 150, 250, 400 keV, and ion injection dose = 5×10^{17}, 2×10^{18}, 4×10^{18} cm^{-2}, followed by a heat treatment at 1,200 °C for 36 hours. With an oxygen profile such as that shown in Fig. 6(b), SOI (silicon on insulator) on SiO_2 film having a thickness of about 1.3 μm was realized. A 20 V driving circuit can be made by forming a CMOS inverter on this SIMOX substrate.

Example 5

[0065] The active matrix substrate of an active matrix type of liquid crystal display was manufactured by forming a polycrystalline or amorphous Si layer on a transparent substrate and by processing a necessary portion thereof by laser

annealing so that the processed portion is changed into a monocrystal. Fig. 7(a) is a plan view of this display. A display portion 72 is formed at the center of the substrate and is surrounded by a drive circuit portion 71. Chips integrated in an active matrix and a circuit for driving the matrix are provided on a device region 74 formed in an amorphous region 73. A laser light source used for laser annealing is of a high output (5 to 1,000 mW) type using a helium neon lamp as a light source. In the display in accordance with this example, only the drive circuit is required to have a high-speed switching operation. Therefore, only the drive circuit portion is scanned with the laser light source, as illustrated. The scanned portion is changed into a monocrystal region where the carrier mobility is the same as that in ordinary monocrystal Si, thereby enabling high-speed driving. The manufacturing cost is increased by the laser annealing process. However, the increase in the manufacturing cost is limited by setting a necessary minimum processed region as described above. It is thereby possible to manufacture a high-integration high-resolution liquid crystal display having two hundred thousand or more pixels.

Example 6 (3rd Embodiment)

[0066] Fig. 8 shows an example of an active matrix substrate of an active matrix liquid crystal display device produced in accordance with the present invention. In this embodiment, a drive circuit portion 71 is formed on a thick SiO_2 film 83 (having a thickness of 1 µm (10, 000 Å) for example), enabling driving of $V_{DD} - V_{SS} = 14$ V. A display portion 72 in which transistors serving as switching devices for applying voltages to liquid crystal cells are arranged in the form of a matrix is formed on a thin SiO_2 film 82. A monocrystal Si substrate 81 at the back side of the display portion 72 is partially removed by wet etching, and a space thereby formed is filled with back packing (silicone rubber) 84 for reinforcement. This packing is almost transparent and allows back light from under to pass in order to efficiently illuminate the display portion.

[0067] Only PMOS transistors are used as switching devices in the display portion. The back packing 84 has an insulating property. Therefore, even if there are movable ions (ordinarily, positive ions) in the back packing, the parasitic PMOS transistor does not operate by this charge.

[0068] Thus, an unnecessary increase in the SiO_2 film is limited to reduce stresses remaining in the SiO_2 film and the device region after cutting-out of the monocrystal silicon substrate. It is thereby possible to avoid an arrangement of liquid crystal cells on the outer device region and to improve image qualities.

[0069] As described above, in the semiconductor device produced in accordance with the present invention, a leak current, relating to the problem of the conventional SIMOX art, can be prevented by controlling the film thickness of the implant formed insulation layer. The semiconductor device can perform high speed driving with a high power supply voltage. The liquid crystal display device produced according to the present invention can be designed for high-resolution high-image-quality image display.

Claims

1. A method of producing a thin-film CMOS inverter circuit comprising:

a monocrystalline silicon bulk semiconductor substrate (1);
an insulation layer (2) on said semiconductor substrate;
a thin-film Si layer (4 to 7,10,11,12,12',13,13') on said insulation layer;
a thin-film NMOS transistor (16) having a source (4,12) and a drain (5,15) in a first isolated monocrystal region (4,5,10,12,12') of said thin-film Si layer, a source electrode (14), a drain electrode (15), and an insulated gate electrode (9);
a thin-film PMOS transistor (17) having a source (7,13') and a drain (6,13) in a second isolated monocrystal region (6,7,11,13,13') of said thin-film Si layer, a source electrode (14'), a drain electrode (15') and an insulated gate electrode (9');
a common input electrode connected to said gate electrode of said NMOS transistor and to said gate electrode of said PMOS transistor;
a common output electrode connected to said drain electrode of said NMOS transistor and to said drain electrode of said PMOS transistor;
a low-voltage power supply, connected to said source electrode of said NMOS transistor, to supply a first voltage, V_{SS} volts, thereto; and
a high-voltage power supply connected to said source electrode of said PMOS transistor to supply a second voltage, V_{DD} volts, thereto; wherein
the thickness T_{BOX} of said insulation (2) satisfies a relationship expressed by the following expression:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

where

$$K_1 \equiv \epsilon_{BOX}^{-1} (Q_{BN} + Q_{BP}),$$

$K_2 = 2\phi_{FN} + 2\phi_{FP} - 1.03$ Volts, ϵ_{BOX} is a dielectric constant of said base insulation layer (2), Q_{BN} and Q_{BP} are bulk charges when the widths of depletion layers of said NMOS and PMOS transistors (16,17) are maximized and are expressed in units of Coulombs/cm^2, and ϕ_{FN} and ϕ_{FP} are pseudo Fermi potentials of said NMOS and PMOS transistors (16,17) expressed in volts, whereby parasitic MOS transistors, having said semiconductor substrate (1) as a common gate electrode, said insulation layer (2) as gate insulation, said source (4) and said drain (5) of said NMOS transistor (16) and said source (7) and said drain (6) of said PMOS transistor (17), inherent in said circuit, are inoperable;
which method is performed by:
providing a monocrystalline silicon bulk semiconductor wafer;
implanting oxygen ions in said bulk semiconductor wafer by irradiating the surface thereof with double charged oxygen ions and performing an anneal heat treatment, thereby forming the insulation layer (2) of SiO_2 which separates a surface layer of said wafer, which is to provide at least a lower part of the thin film Si layer (4-7,10,11,12,12',13,13') from a remainder portion of said wafer, namely the monocrystalline silicon bulk semiconductor substrate (1), the thickness of said insulation layer (2) thus formed being about 1 µm ; producing the thin-film NMOS transistor (16) and the thin-film PMOS transistor (17) in and upon respective first and second isolated monocrystal regions (4,5,10,12,12' and 6,7,11,13,13') of said thin film Si layer,;
connecting the respective gates (9,9') to a common input electrode, and connecting the respective drains (15,15') to a common output electrode ; and providing the low-voltage power supply and the high-voltage power supply and connecting them to the respective sources of said NMOS and PMOS transistors.

2. A method of producing a thin-film CMOS inverter circuit comprising:

a monocrystalline silicon bulk semiconductor substrate (1);
an insulation layer (2) on said semiconductor substrate;
a thin-film Si layer (4 to 7,10,11,12,12',13,13') on said insulation layer;
a thin-film NMOS transistor (16) having a source (4,12) and a drain (5,15) in a first isolated monocrystal region (4,5,10,12,12') of said thin-film Si layer, a source electrode (14), a drain electrode (15), and an insulated gate electrode (9);
a thin-film PMOS transistor (17) having a source (7,13') and a drain (6,13) in a second isolated monocrystal region (6,7,11,13,13') of said thin-film Si layer, a source electrode (14'), a drain electrode (15') and an insulated gate electrode (9');
a common input electrode connected to said gate electrode of said NMOS transistor and to said gate electrode of said PMOS transistor;
a common output electrode connected to said drain electrode of said NMOS transistor and to said drain electrode of said PMOS transistor;
a low-voltage power supply, connected to said source electrode of said NMOS transistor, to supply a first voltage, V_{SS} volts, thereto; and
a high-voltage power supply connected to said source electrode of said PMOS transistor to supply a second voltage, V_{DD} volts, thereto; wherein
the thickness T_{BOX} of said insulation (2) satisfies a relationship expressed by the following expression:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

where

$$K_1 \equiv \epsilon_{BOX}^{-1} (Q_{BN} + Q_{BP}),$$

$K_2 = 2\phi_{FN} + 2\phi_{FP} - 1.03$ Volts, ϵ_{BOX} is a dielectric constant of said base insulation layer (2), Q_{BN} and Q_{BP} are bulk charges when the widths of depletion layers of said NMOS and PMOS transistors (16,17) are maximized and are expressed in units of Coulombs/cm^2, and ϕ_{FN} and ϕ_{FP} are pseudo Fermi potentials of said

NMOS and PMOS transistors (16,17) expressed in volts, whereby parasitic MOS transistors, having said semiconductor substrate (1) as a common gate electrode, said insulation layer (2) as gate insulation, said source (4) and said drain (5) of said NMOS transistor (16) and said source (7) and said drain (6) of said PMOS transistor (17), inherent in said circuit, are inoperable;
which method is performed by :

providing a monocrystalline silicon bulk semiconductor wafer ;
implanting oxygen ions in said bulk semiconductor wafer by irradiating the surface thereof with oxygen ions for three exposures performed at three different implant energies, and annealing by heat treatment, thereby forming the insulation layer (2) of SiO_2 which separates a surface layer of said wafer, which is to provide at least a lower part of the thin film Si layer (4-7,10,11,12,12',13,13') from a remainder portion of said wafer, namely the monocrystalline silicon bulk semiconductor substrate (1), the thickness of said insulation layer (2) thus formed being about 1.3µm; producing the thin-film NMOS transistor (16) and the thin-film PMOS transistor (17) in and upon respective first and second isolated monocrystal regions (4,5,10,12,12' and 6,7,11,13,13') of said thin film Si layer ;
connecting the respective gates (9,9') to a common input electrode, a connecting the respective drains (15,15') to a common output electrode ; and providing the low-voltage power supply and the high-voltage power supply and connecting them to the respective sources of said NMOS and PMOS transistors.

3. A method of producing the active matrix substrate (81-85) of a liquid crystal display device having both a peripheral drive circuit portion (71) and an active matrix display portion (72) which method includes performing the method of producing a thin-film CMOS inverter circuit according to either of claims 1 or 2, said thin film NMOS and PMOS transistors of said thin film CMOS inverter circuit being located at the periphery of the SOI substrate formed of said monocrystalline silicon bulk semiconductor substrate, insulation layer and thin film Si layer, and provided as part of a peripheral drive circuit portion (71) of the active matrix substrate of the liquid crystal display device ; and also includes steps of :

producing the active matrix display portion in and upon said thin-film Si layer, which portion has PMOS pixel switches ; removing the portion of the monocrystal Si bulk substrate disposal between said active matrix display portion (72) of said thin-film Si layer (5) and the back surface of said monocrystal Si bulk substrate, thinning the portion of the insulation layer (83-82) exposed by removal of said portion of the monocrystal Si bulk substrate, and in-filling the void formed by said removal and said thinning with a substantially transparent back packing material (84) for reinforcement.

Patentansprüche

1. Verfahren zur Herstellung einer Dünnfilm-CMOS-Inverterschaltung mit

einem massiven einkristallinen Siliciumhalbleitersubstrat (1);
einer Isolationsschicht (2) auf dem erwähnten Halbleitersubstrat;
einer Dünnfilm-Si-Schicht (4 bis 7, 10, 11, 12, 12', 13, 13') auf der erwähnten Isolationsschicht;
einem Dünnfilm-NMOS-Transistor (16), der eine Source (4, 12) und einen Drain (5, 12') in einem ersten isolierten Einkristallbereich (4, 5, 10, 12, 12') der erwähnten Dünnfilm-Si-Schicht, eine Sourceelektrode (14), eine Drainelektrode (15) und eine isolierte Gateelektrode (9) hat;
einem Dünnfilm-PMOS-Transistor (17), der eine Source (7, 13') und einen Drain (6, 13) in einem zweiten isolierten Einkristallbereich (6, 7, 11, 13, 13') der erwähnten Dünnfilm-Si-Schicht, eine Sourceelektrode (14'), eine Drainelektrode (15') und eine isolierte Gateelektrode (9') hat;
einer gemeinsamen Eingangselektrode, die mit der erwähnten Gateelektrode des erwähnten NMOS-Transistors und mit der erwähnten Gateelektrode des erwähnten PMOS-Transistors verbunden ist;
einer gemeinsamen Ausgangselektrode, die mit der erwähnten Drainelektrode des erwähnten NMOS-Transistors und mit der erwähnten Drainelektrode des erwähnten PMOS-Transistors verbunden ist;
einem Stromversorgungsgerät für niedrige Spannung, das mit der erwähnten Sourceelektrode des erwähnten NMOS-Transistors verbunden ist, um diese mit einer ersten Spannung (V_{SS} Volt) zu versorgen; und
einem Stromversorgungsgerät für hohe Spannung, das mit der erwähnten Sourceelektrode des erwähnten PMOS-Transistors verbunden ist, um diese mit einer zweiten Spannung (V_{DD} Volt) zu versorgen; wobei
die Dicke T_{BOX} der erwähnten Isolation (2) eine Beziehung erfüllt, die durch den folgenden Ausdruck ausgedrückt wird:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1,$$

worin

$$K_1 = \varepsilon_{BOX}^{-1} \ (Q_{BN} + Q_{BP}),$$

$K_2 = 2\phi_{FN} + 2\phi_{FP} - 1{,}03$ Volt, ε_{BOX} die Dielektrizitätskonstante der erwähnten Basisisolationsschicht (2) ist, Q_{BN} und Q_{BP} Volumenladungen in dem Fall sind, dass die Breiten der Verarmungsschichten des erwähnten NMOS- und PMOS-Transistors (16, 17) maximiert sind, und in Einheiten von Coulomb/cm^2 ausgedrückt werden, und ϕ_{FN} und ϕ_{FP} Pseudo-Fermi-Potentiale des erwähnten NMOS- und PMOS-Transistors (16, 17) sind, die in Volt ausgedrückt werden, wodurch der erwähnten Schaltung eigene parasitäre MOS-Transistoren, die das erwähnte Halbleitersubstrat (1) als gemeinsame Gateelektrode, die erwähnte Isolationsschicht (2) als Gateisolation, die erwähnte Source (4) und den erwähnten Drain (5) des erwähnten NMOS-Transistors (16) und die erwähnte Source (7) und den erwähnten Drain (6) des erwähnten PMOS-Transistors (17) haben, unwirksam sind;

wobei dieses Verfahren dadurch durchgeführt wird, dass

ein massiver einkristalliner Siliciumhalbleiterwafer bereitgestellt wird;

in den erwähnten massiven Siliciumhalbleiterwafer Sauerstoffionen implantiert werden, indem seine Oberfläche mit doppelt aufgeladenen Sauerstoffionen bestrahlt und eine Ausheilungswärmebehandlung durchgeführt wird, wodurch die aus SiO_2 bestehende Isolationsschicht (2) gebildet wird, die eine Oberflächenschicht des erwähnten Wafers, die mindestens einen unteren Teil der Dünnfilm-Si-Schicht (4 bis 7, 10, 11, 12, 12', 13, 13') bereitzustellen hat, von einem restlichen Teil des erwähnten Wafers, nämlich von dem massiven einkristallinen Siliciumhalbleitersubstrat (1), trennt, wobei die Dicke der erwähnten auf diese Weise gebildeten Isolationsschicht (2) etwa 1 µm beträgt;

der Dünnfilm-NMOS-Transistor (16) und der Dünnfilm-PMOS-Transistor (17) in und auf dem ersten bzw. dem zweiten isolierten Einkristallbereich (4, 5, 10, 12, 12' und 6, 7, 11, 13, 13') der erwähnten Dünnfilm-Si-Schicht hergestellt werden;

die jeweiligen Gateelektroden (9, 9') mit einer gemeinsamen Eingangselektrode verbunden werden und die jeweiligen Drainelektroden (15, 15') mit einer gemeinsamen Ausgangselektrode verbunden werden und

das Stromversorgungsgerät für niedrige Spannung und das Stromversorgungsgerät für hohe Spannung bereitgestellt und mit der Sourceelektrode des erwähnten NMOS- bzw. des erwähnten PMOS-Transistors verbunden werden.

2. Verfahren zur Herstellung einer Dünnfilm-CMOS-Inverterschaltung mit

einem massiven einkristallinen Siliciumhalbleitersubstrat (1);

einer Isolationsschicht (2) auf dem erwähnten Halbleitersubstrat;

einer Dünnfilm-Si-Schicht (4 bis 7, 10, 11, 12, 12', 13, 13') auf der erwähnten Isolationsschicht;

einem Dünnfilm-NMOS-Transistor (16), der eine Source (4, 12) und einen Drain (5, 12') in einem ersten isolierten Einkristallbereich (4, 5, 10, 12, 12') der erwähnten -Dünnfilm-Si-Schicht, eine Sourceelektrode (14), eine Drainelektrode (15) und eine isolierte Gateelektrode (9) hat;

einem Dünnfilm-PMOS-Transistor (17), der eine Source (7, 13') und einen Drain (6, 13) in einem zweiten isolierten Einkristallbereich (6, 7, 11, 13, 13') der erwähnten Dünnfilm-Si-Schicht, eine Sourceelektrode (14'), eine Drainelektrode (15') und eine isolierte Gateelektrode (9') hat;

einer gemeinsamen Eingangselektrode, die mit der erwähnten Gateelektrode des erwähnten NMOS-Transistors und mit der erwähnten Gateelektrode des erwähnten PMOS-Transistors verbunden ist;

einer gemeinsamen Ausgangselektrode, die mit der erwähnten Drainelektrode des erwähnten NMOS-Transistors und mit der erwähnten Drainelektrode des erwähnten PMOS-Transistors verbunden ist;

einem Stromversorgungsgerät für niedrige Spannung, das mit der erwähnten Sourceelektrode des erwähnten NMOS-Transistors verbunden ist, um diese mit einer ersten Spannung (V_{SS} Volt) zu versorgen; und

einem stromversorgungsgerät für hohe Spannung, das mit der erwähnten Sourceelektrode des erwähnten PMOS-Transistors verbunden ist, um diese mit einer zweiten Spannung (V_{DD} Volt) zu versorgen; wobei

die Dicke T_{BOX} der erwähnten Isolation (2) eine Beziehung erfüllt, die durch den folgenden Ausdruck ausgedrückt wird:

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1,$$

worin

$$K_1 \equiv \varepsilon_{BOX}^{-1} \ (Q_{BN} + Q_{BP}),$$

$K_2 = 2\phi_{FN} + 2\phi_{FP}$ - 1,03 Volt, ε_{BOX} die Dielektrizitätskonstante der erwähnten Basisisolationsschicht (2) ist, Q_{BN} und Q_{BP} Volumenladungen in dem Fall sind, dass die Breiten der Verarmungsschichten des erwähnten NMOS- und PMOS-Transistors (16, 17) maximiert sind, und in Einheiten von Coulomb/cm^2 ausgedrückt werden, und ϕ_{FN} und ϕ_{FP} Pseudo-Fermi-Potentiale des erwähnten NMOS- und PMOS-Transistors (16, 17) sind, die in Volt ausgedrückt werden, wodurch der erwähnten Schaltung-eigene parasitäre MOS-Transistoren, die das erwähnte Halbleitersubstrat (1) als gemeinsame Gateelektrode, die erwähnte Isolationsschicht (2) als Gateisolation, die erwähnte Source (4) und den erwähnten Drain (5) des erwähnten NMOS-Transistors (16) und die erwähnte Source (7) und den erwähnten Drain (6) des erwähnten PMOS-Transistors (17) haben, unwirksam sind;

wobei dieses Verfahren dadurch durchgeführt wird, dass

ein massiver einkristalliner Siliciumhalbleiterwafer bereitgestellt wird;

in den erwähnten massiven Siliciumhalbleiterwafer Sauerstoffionen implantiert werden, indem seine Oberfläche einer dreimaligen Bestrahlung mit Sauerstoffionen ausgesetzt wird, die mit drei verschiedenen Implantationsenergien durchgeführt wird, und eine Ausheilung durch Wärmebehandlung durchgeführt wird, wodurch die aus SiO_2 bestehende Isolationsschicht (2) gebildet wird, die eine Oberflächenschicht des erwähnten Wafers, die mindestens einen unteren Teil der Dünnfilm-Si-Schicht (4 bis 7, 10, 11, 12, 12', 13, 13') bereitzustellen hat, von einem restlichen Teil des erwähnten Wafers, nämlich von dem massiven einkristallinen Siliciumhalbleitersubstrat (1), trennt, wobei die Dicke der erwähnten auf diese Weise gebildeten Isolationsschicht (2) etwa 1,3 µm beträgt;

der Dünnfilm-NMOS-Transistor (16) und der Dünnfilm-PMOS-Transistor (17) in und auf dem ersten bzw. dem zweiten isolierten Einkristallbereich (4, 5, 10, 12, 12' und 6, 7, 11, 13, 13') der erwähnten Dünnfilm-Si-Schicht hergestellt werden;

die jeweiligen Gateelektroden (9, 9') mit einer gemeinsamen Eingangselektrode verbunden werden und die jeweiligen Drainelektroden (15, 15') mit einer gemeinsamen Ausgangselektrode verbunden werden und

das Stromversorgungsgerät für niedrige Spannung und das Stromversorgungsgerät für hohe Spannung bereitgestellt und mit der Sourceelektrode des erwähnten NMOS- bzw. des erwähnten PMOS-Transistors verbunden werden.

3. Verfahren zur Herstellung des Aktivmatrixsubstrats (81 bis 85) eines Flüssigkristallanzeigegeräts, das einen peripheren Ansteuerschaltungsbereich (71) und einen Aktivmatrixanzeigebereich (72) hat, wobei dieses Verfahren die Durchführung des Verfahrens nach Anspruch 1 oder 2 zur Herstellung einer Dünnfilm-CMOS-Inverterschaltung einschließt, wobei der erwähnte Dünnfilm-NMOS-Transistor und der erwähnte Dünnfilm-PMOS-Transistor der erwähnten Dünnfilm-CMOS-Inverterschaltung an der Peripherie des SOI-Substrats, das aus dem erwähnten massiven einkristallinen Siliciumhalbleitersubstrat, der erwähnten Isolationsschicht und der erwähnten Dünnfilm-Si-Schicht gebildet wird, angeordnet und als Teil eines peripheren Ansteuerschaltungsbereichs (71) des Aktivmatrixsubstrats des Flüssigkristallanzeigegeräts bereitgestellt werden, und auch die folgenden Schritte einschließt:

Herstellung des Aktivmatrixanzeigebereichs in und auf der erwähnten Dünnfilm-Si-Schicht, wobei dieser Bereich PMOS-Bildelementschalter hat;

Entfernung des zwischen dem erwähnten Aktivmatrixanzeigebereich (72) der erwähnten Dünnfilm-Si-Schicht (85) und der Rückseite des erwähnten massiven einkristallinen Si-Substrats angeordneten Bereichs des massiven einkristallinen Si-Substrats;

Verdünnung des durch Entfernung des erwähnten Bereichs des massiven einkristallinen Si-Substrats freigelegten Bereichs der Isolationsschicht (83) und

Auffüllung des durch die erwähnte Entfernung und die erwähnte Verdünnung gebildeten Hohlraums mit einem im wesentlichen lichtdurchlässigen Auffüllungsmaterial (84) zur Verstärkung.

Revendications

1. Procédé de fabrication d'un circuit inverseur CMOS à couche mince, comprenant :

un substrat semiconducteur massif (1) en silicium monocristallin;
une couche d'isolation (2) sur le substrat semiconducteur;

une couche mince de Si (4 à 7, 10, 11, 12, 12', 13, 13') sur la couche d'isolation;
un transistor NMOS à couche mince (16) ayant une source (4, 12) et un drain (5, 15) dans une première région de monocristal isolée (4, 5, 10, 12, 12') de la couche mince de Si, une électrode de source (14), une électrode de drain (15) et une électrode de grille isolée (9);
un transistor PMOS à couche mince (17) ayant une source (7, 13') et un drain (6, 13) dans une seconde région de monocristal isolée (6, 7, 11, 13, 13') de la couche mince de Si, une électrode de source (14'), une électrode de drain (15') et une électrode de grille isolée (9');
une électrode d'entrée commune connectée à l'électrode de grille du transistor NMOS et à l'électrode de grille du transistor PMOS;
une électrode de sortie commune connectée à l'électrode de drain du transistor NMOS et à l'électrode de drain du transistor PMOS;
une alimentation de faible tension, connectée à l'électrode de source du transistor NMOS, pour lui appliquer une première tension, de V_{SS} volts; et
une alimentation de tension élevée connectée à l'électrode de source du transistor PMOS pour lui appliquer une seconde tension, de V_{DD} volts; dans lequel
l'épaisseur T_{BOX} de l'isolation (2) vérifie une relation exprimée par l'expression :

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

dans laquelle

$$K_1 \equiv \varepsilon_{BOX}^{-1} (Q_{BN} + Q_{BP}),$$

$K_2 = 2\phi_{FN} + 2\phi_{FP} - 1{,}03$ volts, ε_{BOX} est une constante diélectrique de la couche d'isolation de base (2), Q_{BN} et Q_{BP} sont des charges de substrat lorsque les largeurs des couches de désertion des transistors NMOS et PMOS (16, 17) sont maximisées, et s'expriment en coulombs/cm^2, et ϕ_{FN} et ϕ_{FP} sont des pseudo-potentiels de Fermi des transistors NMOS et PMOS (16, 17), exprimés en volts, grâce à quoi des transistors MOS parasites, ayant le substrat semiconducteur (1) en tant qu'électrode de grille commune, la couche d'isolation (2) en tant qu'isolation de grille, la source (4) et le drain (5) du transistor NMOS (16) et la source (7) et le drain (6) du transistor PMOS (17), qui sont inhérents dans le circuit, ne peuvent pas fonctionner;
ce procédé étant accompli par les opérations suivantes :
on fournit une tranche de semiconducteur massif en silicium monocristallin;
on implante des ions d'oxygène dans ladite tranche de semiconducteur massif, par irradiation de la surface de celle-ci avec des ions d'oxygène doublement chargés, et on effectue un traitement thermique de recuit, pour former ainsi la couche d'isolation (2) en SiO_2 qui sépare une couche de surface de ladite tranche, qui doit constituer au moins une partie inférieure de la couche mince de Si (4-7, 10, 11, 12, 12', 13, 13'), d'une partie restante de la tranche, c'est-à-dire le substrat semiconducteur massif (1) en silicium monocristallin, l'épaisseur de la couche d'isolation (2) ainsi formée étant d'environ 1 µm;
on produit le transistor NMOS à couche mince (16) et le transistor PMOS à couche mince (17) dans et sur des première et seconde régions de monocristal isolées respectives (4, 5, 10, 12, 12' et 6, 7, 11, 13, 13') de la couche mince de Si;
on connecte les grilles respectives (9, 9') à une électrode d'entrée commune, et on connecte les drains respectifs (15, 15') à une électrode de sortie commune; et
on fournit l'alimentation de faible tension et l'alimentation de tension élevée et on les connecte aux sources respectives des transistors NMOS et PMOS.

2. Procédé de fabrication d'un circuit inverseur CMOS à couche mince, comprenant :

un substrat semiconducteur massif (1) en silicium monocristallin;
une couche d'isolation (2) sur le substrat semiconducteur;
une couche mince de Si (4 à 7, 10, 11, 12, 12', 13, 13') sur la couche d'isolation;
un transistor NMOS à couche mince (16) ayant une source (4, 12) et un drain (5, 15) dans une première région de monocristal isolée (4, 5, 10, 12, 12') de la couche mince de Si, une électrode de source (14), une électrode de drain (15) et une électrode de grille isolée (9);
un transistor PMOS à couche mince (17) ayant une source (7, 13') et un drain (6, 13) dans une seconde région de monocristal isolée (6, 7, 11, 13, 13') de la couche mince de Si, une électrode de source (14'), une électrode de drain (15') et une électrode de grille isolée (9');

une électrode d'entrée commune connectée à l'électrode de grille du transistor NMOS et à l'électrode de grille du transistor PMOS;
une électrode de sortie commune connectée à l'électrode de drain du transistor NMOS et à l'électrode de drain du transistor PMOS;
une alimentation de faible tension, connectée à l'électrode de source du transistor NMOS, pour lui appliquer une première tension, de V_{SS} volts; et
une alimentation de tension élevée connectée à l'électrode de source du transistor PMOS pour lui appliquer une seconde tension, de V_{DD} volts; dans lequel
l'épaisseur T_{BOX} de l'isolation (2) vérifie une relation exprimée par l'expression :

$$T_{BOX} > (V_{DD} - V_{SS} - K_2)/K_1$$

dans laquelle

$$K_1 = \varepsilon_{BOX}^{-1} (Q_{BN} + Q_{BP}),$$

$K_2 = 2\phi_{FN} + 2\phi_{FP} - 1{,}03$ volts, ε_{BOX} est une constante diélectrique de la couche d'isolation de base (2), Q_{BN} et Q_{BP} sont des charges de substrat lorsque les largeurs des couches de désertion des transistors NMOS et PMOS (16, 17) sont maximisées, et s'expriment en coulombs/cm^2, et ϕ_{FN} et ϕ_{FP} sont des pseudo-potentiels de Fermi des transistors NMOS et PMOS (16, 17), exprimés en volts, grâce à quoi des transistors MOS parasites, ayant le substrat semiconducteur (1) en tant qu'électrode de grille commune, la couche d'isolation (2) en tant qu'isolation de grille, la source (4) et le drain (5) du transistor NMOS (16) et la source (7) et le drain (6) du transistor PMOS (17), qui sont inhérents dans le circuit, ne peuvent pas fonctionner;
ce procédé étant accompli par les opérations suivantes :
on fournit une tranche de semiconducteur massif en silicium monocristallin;
on implante des ions d'oxygène dans ladite tranche de semiconducteur massif, par irradiation de la surface de celle-ci avec des ions d'oxygène pour trois expositions effectuées à trois énergies d'implantation différentes, et on effectue un recuit par traitement thermique, pour former ainsi la couche d'isolation (2) en SiO_2 qui sépare une couche de surface de ladite tranche, qui doit constituer au moins une partie inférieure de la couche mince de Si (4-7, 10, 11, 12, 12', 13, 13'), d'une partie restante de la tranche, c'est-à-dire le substrat semiconducteur massif (1) en silicium monocristallin, l'épaisseur de la couche d'isolation (2) ainsi formée étant d'environ 1,3 µm;
on produit le transistor NMOS à couche mince (16) et le transistor PMOS à couche mince (17) dans et sur des première et seconde régions de monocristal isolées respectives (4, 5, 10, 12, 12' et 6, 7, 11, 13, 13') de la couche mince de Si;
on connecte les grilles respectives (9, 9') à une électrode d'entrée commune, et on connecte les drains respectifs (15, 15') à une électrode de sortie commune; et
on fournit l'alimentation de faible tension et l'alimentation de tension élevée et on les connecte aux sources respectives des transistors NMOS et PMOS.

3. Procédé pour produire le substrat à matrice active (81-85) d'un dispositif de visualisation à cristal liquide ayant à la fois une partie de circuit d'attaque périphérique (71) et une partie de visualisation à matrice active (72), ce procédé comprenant l'exécution du procédé consistant à produire un circuit inverseur CMOS à couche mince selon l'une quelconque des revendications 1 ou 2, les transistors NMOS et PMOS à couche mince du circuit inverseur CMOS à couche mince se trouvant à la périphérie du substrat SOI formé par le substrat semiconducteur massif en silicium monocristallin, la couche d'isolation et la couche mince de Si, et qui constitue un élément d'une partie de circuit d'attaque périphérique (71) du substrat à matrice active du dispositif de visualisation à cristal liquide, et comprenant également les étapes suivantes :

on produit la partie de visualisation à matrice active dans et sur la couche mince de Si, cette partie ayant des éléments de commutation de pixel PMOS, on enlève la partie du substrat massif en Si monocristallin qui est disposée entre la partie de visualisation à matrice active (72) de la couche mince de Si (85), et la surface arrière du substrat massif en Si monocristallin, on amincit la partie de la couche d'isolation (83-82) qui est mise à nu par l'enlèvement de ladite partie du substrat massif en Si monocristallin, et on remplit le vide formé par l'enlèvement et l'amincissement, avec une matière de remplissage (84) pratiquement transparente, pour le renforcement.

FIG. 1(a)

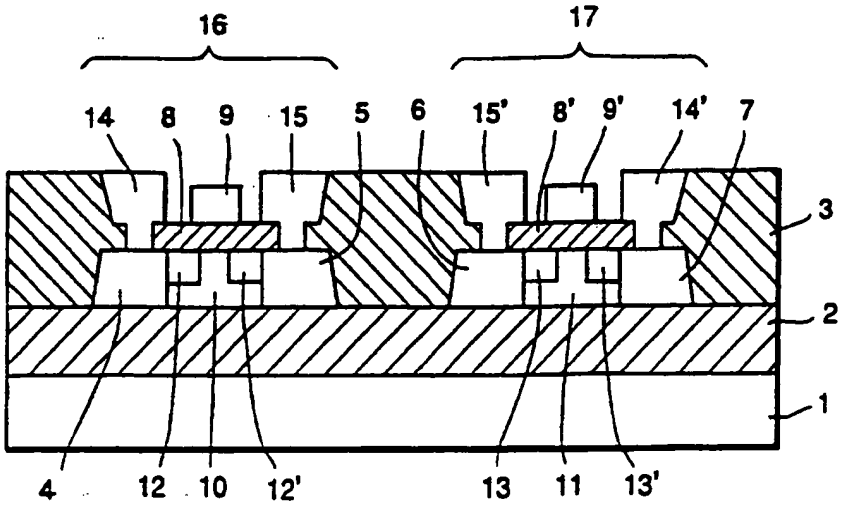

16
17
14
8
9
15
5
6
15'
8'
9'
14'
7
3
2
1
4
12
10
12'
13
11
13'

FIG. 1(b)

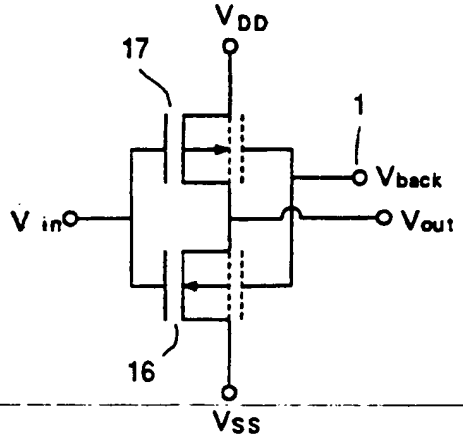

VDD
17
1
Vback
V in
Vout
16
Vss

FIG. 2

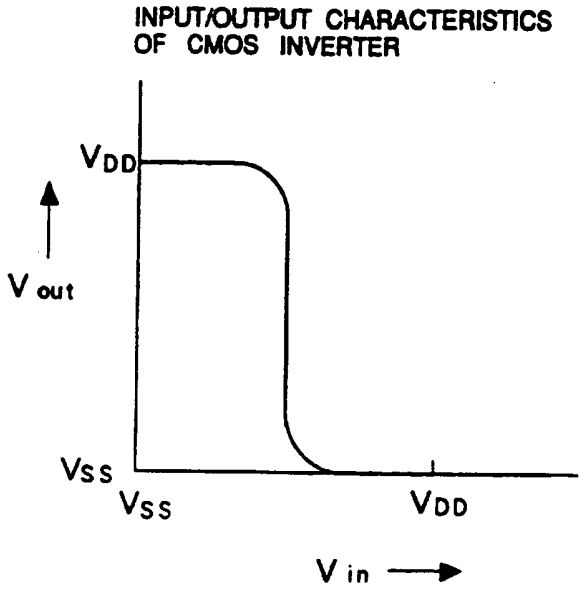

INPUT/OUTPUT CHARACTERISTICS
OF CMOS INVERTER
VDD
V out
VSS
VSS
VDD
V in

FIG. 3

FILM THICKNESS-THRESHOLD VALUE CHARACTERISTICS OF PARASITIC NMOS

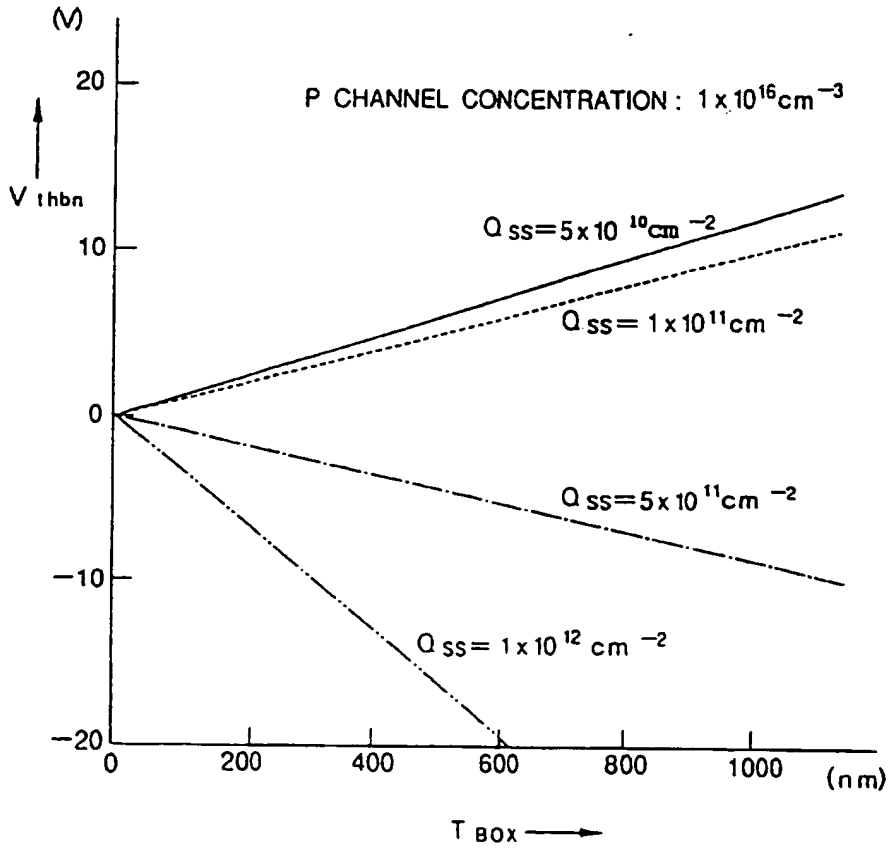


FIG. 4

FILM - THICKNESS - THRESHOLD VALUE CHARACTERISTICS OF PARASITIC PMOS

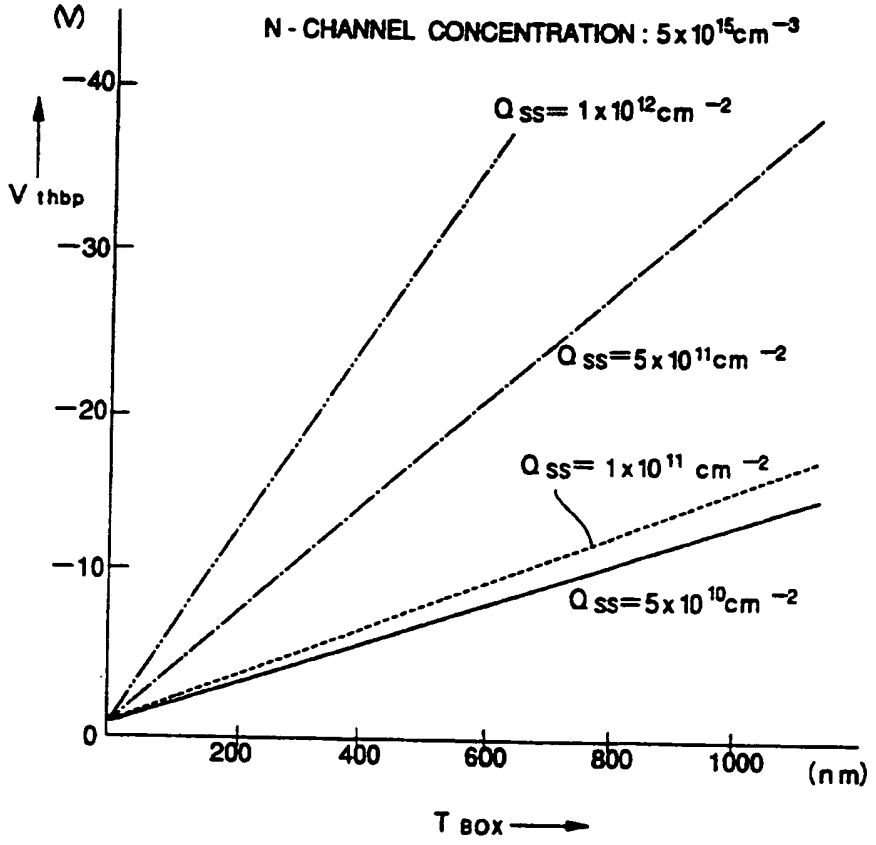
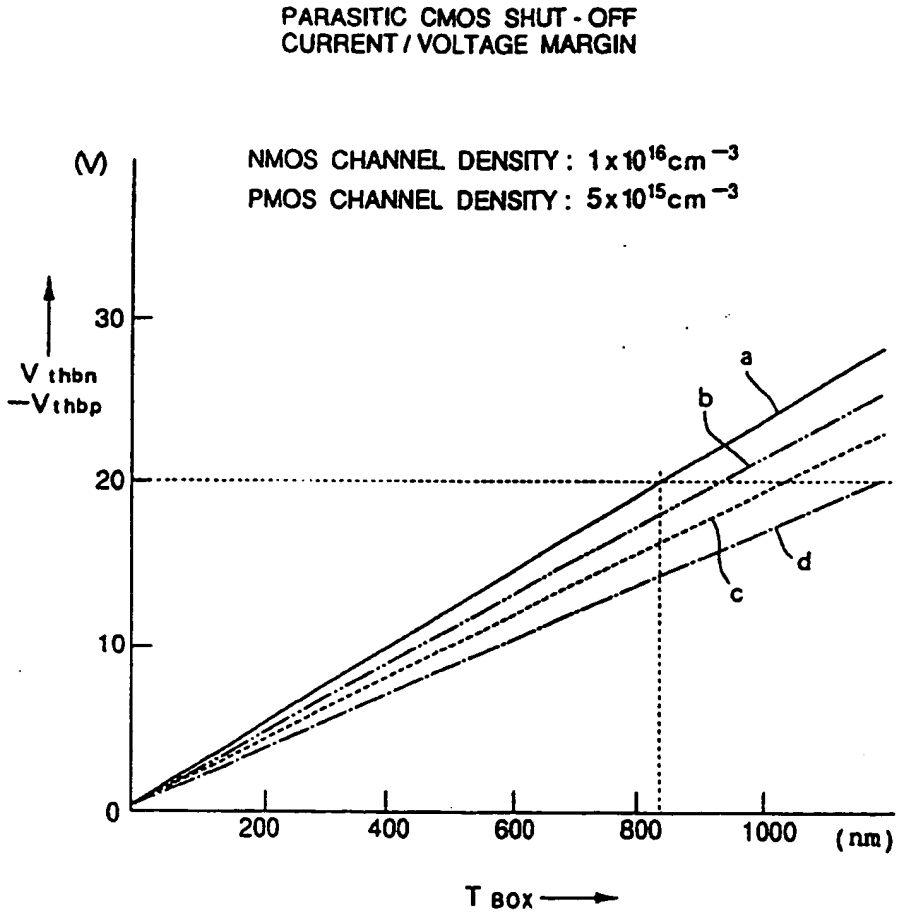


FIG. 5



a : ALLOWABLE CURRENT 1 μA
b : ALLOWABLE CURRENT 10 μA
c : ALLOWABLE CURRENT 100 pA
d : ALLOWABLE CURRENT 1pA

FIG. 6(a)

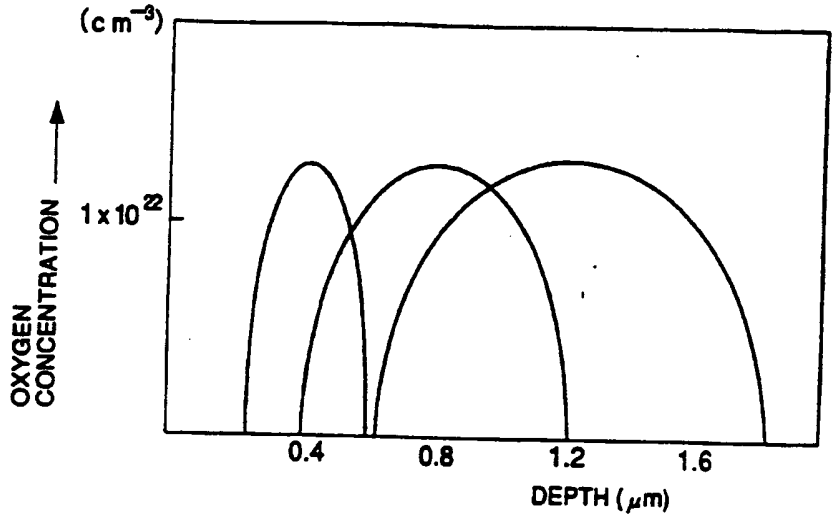

(c m^{-3})
OXYGEN CONCENTRATION
1 x 10^{22}
0.4
0.8
1.2
1.6
DEPTH (μm)

FIG. 6(b)

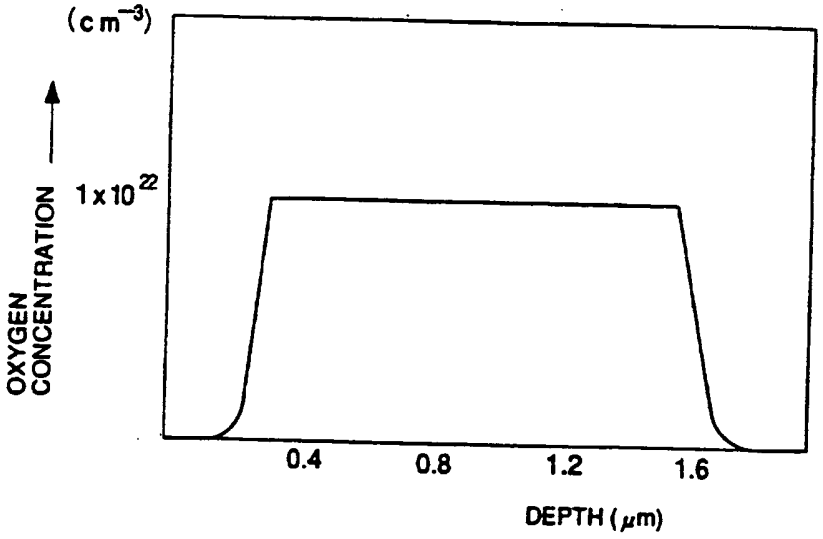

(c m^{-3})
OXYGEN CONCENTRATION
1 x 10^{22}
0.4
0.8
1.2
1.6
DEPTH (μm)

FIG. 7(a)

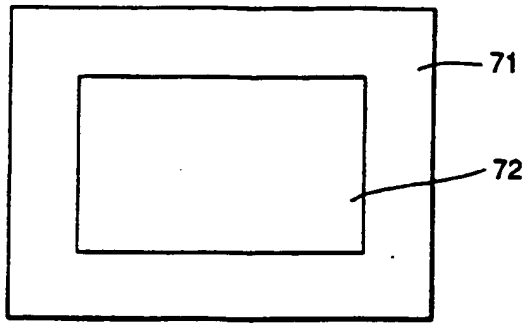


FIG. 7(b)

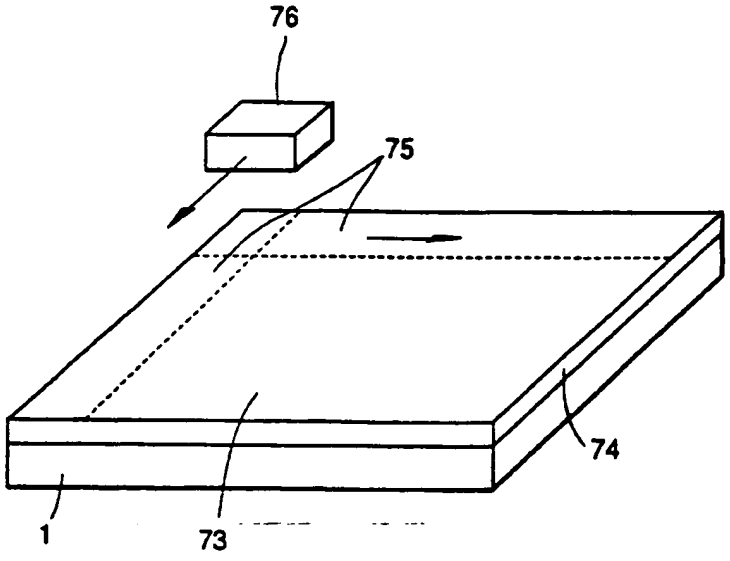


FIG. 8

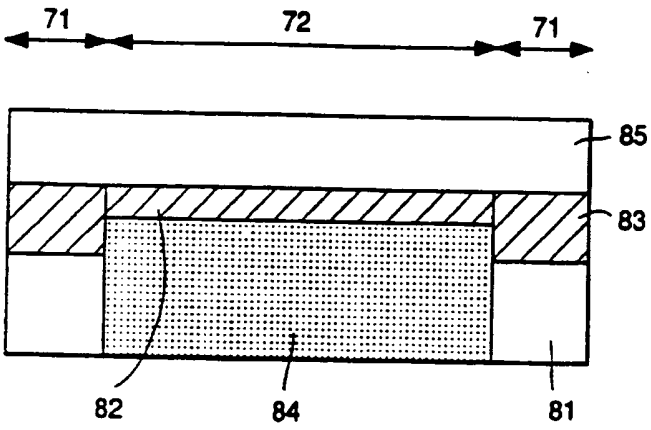
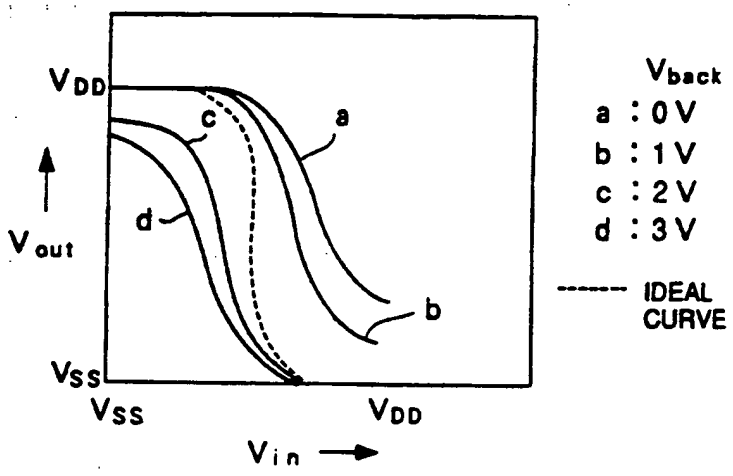


FIG. 9


V_{DD}
V_{out}
V_{SS}
V_{SS}
V_{DD}
V_{in}
a
b
c
d
V_{back}
a : 0 V
b : 1 V
c : 2 V
d : 3 V
IDEAL CURVE